# REAL-TIME DEBUG SUPPORT FOR A DMA DEVICE AND METHOD THEREOF

Abstract of the Disclosure

A data processing system (10) has a debug module (26) that selectively generates one or more debug messages that are specific to a Direct Memory Access (DMA) controller device (16) in the system. A control register(70) enables which of the DMA debug messages are provided. The beginning and end of DMA transfer activity is provided including when minor loop iterations start and complete. Latency information indicating system latency between a channel request and actual initiation of the request for each DMA transfer may also be included in a debug message. One of the debug messages provides periodic status of a predetermined DMA channel under control of a control register (80). At least one of the debug messages implements a watchpoint function, such as indicating when a transfer starts or ends. The debug module may be centralized in the system or distributed among each of predetermined system units.